AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph **[0024]** with the following amended paragraph:

[0024] Figure 3 is a more detailed schematic diagram of the components of the initiator block of Figure 2. Initiator block 124 includes arbitration module 130, which includes multiplexer (mux) 132, state machine 134, and task status and completion circuitry 136. Task status and completion circuitry 136 includes queue 146. It should be appreciated that data lines D_0 through D_n 144 transmit data to arbitrator 130, while corresponding command lines C_0 through C_n 142 transmit commands to state machine 134. The data and corresponding commands originate from the same source. Multiplexer 132 is configured to determine the data which is allowed to pass according to a select signal transmitted over select line 150 and originating from state machine 134. Task status and completion circuitry 136 enables feedback to state machine 134 through depth signal 138 and active signal 140. Through the feedback provided by task status and completion circuitry 136, the amount of bandwidth used for a particular port relative to the corresponding requestor, and the number of total outstanding requests for all ports, is captured in order for state machine 134 to update the bandwidth used by each requestor. This bandwidth indication combines both time spent transferring data as well as any overhead required to setup the memory devices for the transfer. In this way, every cycle in the system is allocated to a particular requestor. The state machine circuitry in [[136]] 134 can also make decisions based upon the overall status of the system. In one embodiment, if the system is not stressed at a certain time, the bandwidth allocation rules can be relaxed without adversely affecting the overall performance of the system. In essence, state machine 134 is

being provided knowledge on the data coming in over data lines D_0 through D_n 144 rather than just seeing the requests from respective command lines C_0 through C_n 142. Accordingly, arbitration module 130 may now take a view of bandwidth factors in addition to fairness factors. Thus, the dotted lines into state machine 134 from respective data lines 144 represent that the state machine is now considering the characteristics of the data in addition to the requestor of the data in the generation of the select signal.

Please replace paragraph **[0025]** with the following amended paragraph:

[0025] Still referring to Figure 3, task status and completion circuitry 136 is configured to deliver the data output from mux 132 to resource [[138]] 148. In one embodiment, resource 148 is placement queue and write data queue block 126 with reference to Figure 2. However, it should be appreciated that resource 148 may be any suitable receiver of the data selected through arbitration module 130, e.g., memory structure, serial port, video board, or other suitable receiver of data, etc. It should be further appreciated that task status and completion circuitry 136 enables feedback to arbitration module 130 on the status of data transferred from the arbitration module, thereby enabling the arbitration scheme to be reactive or adaptive rather than predictive. In one embodiment, the period of time that task status and completion circuitry 136 is working on the data, or a task associated with the data, is translated back into the decision making process for determining which data from the multiple ports to be selected.